***EE 316 – Lab 3 Report: Programming Logic on the Basys3 FPGA Board***

**Ayan Basu [EID: ab73287] (Section: 17760)**

**Saptarshi Mondal [EID: sm72999] (Section: 17760)**

***PART 1*: AND Gate**

***Constraint File***

set\_property PACKAGE\_PIN V17 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN V16 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

set\_property PACKAGE\_PIN U16 [get\_ports {out}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out}]

***Waveform***

Graphical user interface, application, PowerPoint

Description automatically generated

***PART 2*: Sprinkler Valve Controller**

***Constraint File***

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V16 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN W16 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

set\_property PACKAGE\_PIN W13 [get\_ports {e}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {e}]

## LEDs

set\_property PACKAGE\_PIN U16 [get\_ports {d0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d0}]

set\_property PACKAGE\_PIN E19 [get\_ports {d1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d1}]

set\_property PACKAGE\_PIN U19 [get\_ports {d2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d2}]

set\_property PACKAGE\_PIN V19 [get\_ports {d3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d3}]

set\_property PACKAGE\_PIN W18 [get\_ports {d4}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d4}]

set\_property PACKAGE\_PIN U15 [get\_ports {d5}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d5}]

set\_property PACKAGE\_PIN U14 [get\_ports {d6}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d6}]

set\_property PACKAGE\_PIN V14 [get\_ports {d7}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d7}]

***PART 3*: BCD to 7-Segment Display**

***Truth Table, Karnaugh Maps & Gate-Level Design***

(8th bit corresponds to dp, decimal point, which is always 1, or off)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| in | a | b | c | d | e | f | g | out |
| 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | “0” |
| 0001 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | “1” |
| 0010 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | “2” |
| 0011 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | “3” |
| 0100 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | “4” |
| 0101 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | “5” |
| 0110 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | “6” |
| 0111 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | “7” |
| 1000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | “8” |
| 1001 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | “9” |
| 1010 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | “10” |
| 1011 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | “11” |
| 1100 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | “12” |
| 1101 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | “13” |
| 1110 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | “14” |
| 1111 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | “15” |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 0 | 0 |
| 01 | 1 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 |

a = AB + AC + BC’D’ + A’B’C’D

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| B | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 1 | 0 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 |

b = AB + AC + BC’D + BCD’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| C | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 |

c = AB + AC + B’CD’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| D | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 0 | 0 |
| 01 | 1 | 0 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 |

d = AB + AC + BC’D’ + BCD + A’B’C’D



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| E | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 1 | 0 |
| 01 | 1 | 1 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 1 | 1 | 1 |

e = D + BC’+ AC

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| F | 00 | 01 | 11 | 10 |
| 00 | 0 | 1 | 1 | 1 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 |

f = AB + CD + B’C + A’B’D

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| G | 00 | 01 | 11 | 10 |
| 00 | 1 | 1 | 0 | 0 |
| 01 | 0 | 0 | 1 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 1 | 1 |

g = AB + AC + A’B’C’ + BCD

Graphical user interface, application

Description automatically generated with medium confidence

***Simulation***

Graphical user interface, application

Description automatically generated

***BCD\_Display.v (Structural)***

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 09/29/2021 09:13:22 PM

// Design Name:

// Module Name: BCD\_Display

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module BCD\_Seg\_Display(

input i0,

input i1,

input i2,

input i3,

output an0,

output an1,

output an2,

output an3,

output a,

output b,

output c,

output d,

output e,

output f,

output g,

output dp

);

//wires for outputs

wire and\_m0, and\_m1, and\_m2, and\_m3, and\_m4, and\_m5, and\_m6,

and\_m7, and\_m8, and\_m9, and\_m10, and\_m11, and\_m12, and\_m13, and\_m14, and\_m15, not\_i3, not\_i2, not\_i1, not\_i0;

assign an0=1'b0;

assign an1=1'b1;

assign an2=1'b1;

assign an3=1'b1;

assign dp = 1'b1;

//Instantiating Not gates

not n0 (not\_i3, i3);

not n1 (not\_i2, i2);

not n2 (not\_i1, i1);

not n3 (not\_i0, i0);

//make AND gates

and m0 (and\_m0, i3, i2);

and m1 (and\_m1, i3, i1);

and m2 (and\_m2, i2, not\_i1 ,not\_i0);

and m3 (and\_m3, not\_i3, not\_i2, not\_i1, i0);

and m4 (and\_m4, i2, not\_i1, i0);

and m5 (and\_m5, i2, i1, not\_i0);

and m6 (and\_m6, not\_i2, i1, not\_i0);

and m7 (and\_m7, not\_i3, not\_i2, not\_i1, i0);

and m8 (and\_m8, i2, i1, i0);

and m9 (and\_m9, not\_i3, i2, not\_i1);

and m10 (and\_m10, not\_i3, i0);

and m11 (and\_m11, i1, i0);

and m12 (and\_m12, not\_i3, not\_i2, i0);

and m13 (and\_m13,not\_i3, not\_i2, not\_i1);

and m14 (and\_m14, not\_i2, i1);

and m15 (and\_m15, i3, not\_i1, i0);

//set up the OR gates

or agate (a, and\_m0, and\_m1, and\_m2, and\_m3);

or bgate (b, and\_m0, and\_m1, and\_m4, and\_m5);

or cgate (c, and\_m0, and\_m1, and\_m6);

or dgate (d, and\_m0, and\_m1, and\_m2, and\_m7, and\_m8, and\_m15);

or egate (e, and\_m0, and\_m1, and\_m9, and\_m10, i0);

or fgate (f, and\_m0, and\_m1, and\_m11, and\_m12, and\_m14);

or ggate (g, and\_m0, and\_m1, and\_m13, and\_m8);

endmodule

***Tb\_BCD\_Display.v (Structural)***

module tb\_BCD\_structural;

reg i3;

reg i2;

reg i1;

reg i0;

wire a,b,c,d,e,f,g, an0, an1, an2, an3, dp;

BCD\_Seg\_Display uut(

.i3(i3),

.i2(i2),

.i1(i1),

.i0(i0),

.a(a),

.b(b),

.c(c),

.d(d),

.e(e),

.f(f),

.g(g),

.an0 (an0),

.an1 (an1),

.an2 (an2),

.an3 (an3),

.dp (dp)

);

initial begin

i3 = 0;

i2 = 0;

i1 = 0;

i0 = 0;

#50

i3 = 0;

i2 = 0;

i1 = 0;

i0 = 0;

$display ("TC01");

if ({a,b,c,d,e,f,g}!= 7'b0000001)$display ("Result is Wrong");

i3 = 0;

i2 = 0;

i1 = 0;

i0 = 1;

#50

$display ("TC02");

if({a,b,c,d,e,f,g}!= 7'b1001111) $display ("Result is Wrong");

i3 = 0;

i2 = 0;

i1 = 1;

i0 = 0;

#50

$display ("TC03");

if( {a,b,c,d,e,f,g}!= 7'b0010010) $display ("Result is Wrong");

i3 = 0;

i2 = 0;

i1 = 1;

i0 = 1;

#50

$display ("TC04");

if( {a,b,c,d,e,f,g}!= 7'b0000110) $display ("Result is Wrong");

i3 = 0;

i2 = 1;

i1 = 0;

i0 = 0;

#50

$display ("TC05");

if({a,b,c,d,e,f,g}!= 7'b1001100) $display ("Result is Wrong");

i3 = 0;

i2 = 1;

i1 = 0;

i0 = 1;

#50

$display ("TC06");

if({a,b,c,d,e,f,g}!= 7'b0100100) $display ("Result is Wrong");

i3 = 0;

i2 = 1;

i1 = 1;

i0 = 0;

#50

$display ("TC07");

if({a,b,c,d,e,f,g}!= 7'b0100000) $display ("Result is Wrong");

i3 = 0;

i2 = 1;

i1 = 1;

i0 = 1;

#50

$display ("TC08");

if({a,b,c,d,e,f,g}!= 7'b0001111) $display ("Result is Wrong");

i3 = 1;

i2 = 0;

i1 = 0;

i0 = 0;

#50

$display ("TC09");

if({a,b,c,d,e,f,g}!= 7'b0000000) $display ("Result is Wrong");

i3 = 1;

i2 = 0;

i1 = 0;

i0 = 1;

#50

$display ("TC10");

if({a,b,c,d,e,f,g}!= 7'b0001100) $display ("Result is Wrong");

i3 = 1;

i2 = 0;

i1 = 1;

i0 = 0;

#50

$display ("TC11");

if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;

i2 = 0;

i1 = 1;

i0 = 1;

#50

$display ("TC12");

if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;

i2 = 1;

i1 = 0;

i0 = 0;

#50

$display ("TC13");

if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;

i2 = 1;

i1 = 0;

i0 = 1;

#50

$display ("TC14");

if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;

i2 = 1;

i1 = 1;

i0 = 0;

#50

$display ("TC15");

if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

i3 = 1;

i2= 1;

i1 = 1;

i0 = 1;

#50

$display ("TC16");

if({a,b,c,d,e,f,g}!= 7'b1111111) $display ("Result is Wrong");

end

endmodule

***BCD\_Constraint.xdc (Constraint File)***

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {i0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {i0}]

set\_property PACKAGE\_PIN V16 [get\_ports {i1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {i1}]

set\_property PACKAGE\_PIN W16 [get\_ports {i2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {i2}]

set\_property PACKAGE\_PIN W17 [get\_ports {i3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {i3}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {a}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {a}]

set\_property PACKAGE\_PIN W6 [get\_ports {b}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {b}]

set\_property PACKAGE\_PIN U8 [get\_ports {c}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {c}]

set\_property PACKAGE\_PIN V8 [get\_ports {d}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {d}]

set\_property PACKAGE\_PIN U5 [get\_ports {e}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {e}]

set\_property PACKAGE\_PIN V5 [get\_ports {f}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {f}]

set\_property PACKAGE\_PIN U7 [get\_ports {g}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {g}]

set\_property PACKAGE\_PIN V7 [get\_ports dp]

set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U2 [get\_ports {an0}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an0}]

set\_property PACKAGE\_PIN U4 [get\_ports {an1}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an1}]

set\_property PACKAGE\_PIN V4 [get\_ports {an2}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an2}]

set\_property PACKAGE\_PIN W4 [get\_ports {an3}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an3}]